module variables(clk,rst,in,xi,yi,zi);

input clk,rst;

input [7:0]in;

output reg [7:0]xi,yi,zi;

always@(posedge clk)

begin

if(rst)

begin

xi<=8'b0;

yi<=8'b0;

zi<=8'b0;

end

else

begin

if(xi==8'b0 || yi==8'b0 || zi==8'b0)

begin

zi<=yi;

yi<=xi;

xi<=in;

end

end

end

endmodule